WHAT IS CLAIMED IS:

1. A method of manufacturing a flash memory, comprising the steps of:

performing an ion implantation process for adjusting a threshold voltage on a semiconductor substrate;

forming a tunnel oxide film, a first polysilicon film and a pad oxide film on the semiconductor substrate, sequentially;

etching the pad oxide film, the first polysilicon film, the tunnel oxide film and the semiconductor substrate to form a trench defining an active region and a device isolation region;

forming a side wall oxide film on the side wall of the trench while suppressing diffusion of the implanted ion for adjusting the threshold voltage into the device isolation region to the maximum extent;

performing an ion implantation process on the side wall of the trench and the active region adjacent to the device isolation region in order to compensate for ions for adjusting a threshold voltage which have diffused from the active region into the side wall oxide film; and

forming a device isolation film by filling up inside the trench.

2. A method of claim 1, wherein the side wall oxide film is formed by a dry oxidation method at a temperature in the range of 800℃ to 950℃.

3. A method of claim 1, wherein the ion implantation process is performed with a dose of 3E11 ions/㎠ to 1E12 ions/㎠ using an energy of 10Kev to 30Kev at a tilt angle of 0° to 30°.

4. A method of claim 1, wherein the implanted ion for adjusting the threshold voltage is boron.

5. A method of claim 1, after the step of forming a device isolation film, further comprising the steps of;

eliminating the pad nitride film;

forming a second polysilicon film for a floating gate on the structure where the pad nitride film is eliminated;

forming a dielectric film on the structure where the second polysilicon film is formed; and

forming a third polysilicon film for a control gate on the dielectric film.

6. A method of manufacturing a flash memory, comprising the steps of:

performing an ion implantation process for adjusting a threshold voltage on a semiconductor substrate;

forming a tunnel oxide film, a first polysilicon film and a pad oxide film on the semiconductor substrate, sequentially;

etching the pad oxide film, the first polysilicon film, the tunnel oxide film and the semiconductor substrate to form a trench defining an active region and a device isolation region;

performing an annealing process for nitrifying a surface of the trench so as to form a nitride film for preventing the implanted ions for adjusting the threshold voltage from diffusing to the device isolation region;

forming a side wall oxide film on the side wall of the trench while suppressing diffusion of the implanted ion for adjusting the threshold voltage to the device isolation region to the maximum extent; and

forming a device isolation film by filling up inside the trench.

7. A method of claim 6, wherein the side wall oxide film is formed by a dry oxidation method at a temperature in the range of 800℃ to 950℃.

8. A method of claim 6, wherein the annealing process is performed under N_2O atmosphere at a temperature in the range of 800℃ to 900℃.

9. A method of claim 6, after the step of forming a device isolation film, further comprising the steps of;

eliminating the pad nitride film;

forming a second polysilicon film for a floating gate on the structure where the pad nitride film is eliminated;

forming a dielectric film on the structure where the second polysilicon film is formed; and

forming a third polysilicon film for a control gate on the dielectric film.